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Thermal and Supply Voltage Analysis of Optimized Ring Oscillator for Pixel Detector Readout Chip

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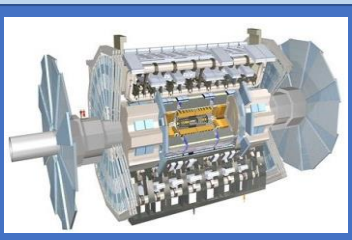
Omar Istaitia[1], Ahmed Bassalat[1]*, Hadil Abualrob[1], Abdenour Lounis[2], Yahya Khwaira[2], Ali Slimani-Cherif[2] & Maurice Cohen-Solal[2]

Abstract: This paper provides a specific study of the upgrade of the ATLAS pixel detector in preparation for the upgrade of the Large Hadron Collider (LHC). The upgrade to High Luminosity-LHC (HL-LHC) is expected to start after the long shutdown in 2025-2027. The scheduled upgrade for ATLAS will be able to efficiently cope with the challenges caused by the high luminosity imposed by the HL-LHC. A new full-silicon Detector Inner Tracker (ITk) will replace the current ATLAS Inner Detector (ID). The ITk pixel detector will consist of more layers than in the current pixel detector. This study focuses on the Ring Oscillator (ROSC) sensors embedded in the ITkPix-V1 Front-End chip of the ATLAS ITk pixel detector. The paper reports the frequency response of the ROSC at various temperatures and voltage supply values. The results showed a high sensitivity of ROSCs frequencies to the applied voltage and the external temperatures which indicates the reliability of the ITkPix-V1 chip for the future ITk pixel modules.



The ATLAS Experiment at CERN.(1)

Keywords: LHC, HL-LHC, ATLAS, ITk, ITkPix-V1, ROSC.

Introduction

A Toroidal LHC Apparatus (ATLAS) is a general multipurpose experiment at one of four interaction points (IP) of the LHC ring. ATLAS is composed of different sub-detectors that are based on various technologies to identify various particles produced from p-p collisions and measure their physical properties.(2) In addition, it extends the search for new physics. The Inner Detector (ID) is the central tracking system of ATLAS and the closest sub-detector to the collision point. It consists of three different systems of sensors immersed in a magnetic field parallel to the beam axis. Two of these systems, Pixel Detector and Semiconductor Tracker (SCT), are silicon detectors, while the third, Radiation Tracker (TRT), is a gas detector. ID serves to reconstruct the track and momentum of electrically charged particles produced in each p-p collision as well as their collision vertices.(3) The pixel detector is used as the first detector around the beam pipe because of its high granularity and radiation hardness.(4) It consists of three barrel layers and three disks per side in addition to an Insertable B-Layer that was recently added as a fourth layer (2014). Figure 1 shows these pixel layers which provide 3-dimensional space points of the particle trajectory.(5)

The HL-LHC will increase particle production, resulting in more tracks passing through the detector layers and increasing occupancy levels. This increased occupancy, in addition to degrading the performance of the detector over time due to radiation damage, resulting from displacement damage in silicon caused by increased particle fluence.(6)

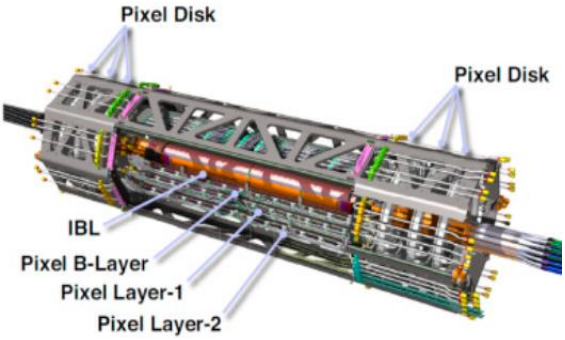


Figure (1): Schematic view of the ATLAS 4-Layer Pixel Detector.

The current silicon tracker requires significant upgrades to cope with the harsh HL-LHC conditions. Many upgrades for different parts of ATLAS detector are planned to maintain performance at current levels despite the increase in occupancy, rate, and radiation damage.

The planned upgrade of the tracking system will replace the current ID with the ITk, a new all-silicon system detector. The ITk contains a more granular and radiation-tolerant pixel detector that has the ability to deal with higher particle density, fluence and high ionizing dose for the HL-LHC.(7)

1 Department of Physics, Faculty of Sciences, An-Najah National University, Nablus, Palestine

*Corresponding Author: ahmed.bassalat@najah.edu

2 IJCLab, Université Paris-Saclay, CNRS/IN2P3, Orsay, France

The ITk pixel detector will be equipped with new pixel modules characterized by larger sensitivity silicon sensors connected to 65 nm CMOS low noise electronics chips. The readout chip provides measurements of physical quantities as deposited charge, in the sensor, time over threshold and houses an inner Ring Oscillator circuits for radiation monitoring. This work is a study of Ring Oscillators optimized for particle tracking in High Energy Colliders.

Principle of Pixel Detector

Pixel detectors are used in the innermost tracking systems of most particle detectors in high-energy physics experiments. A pixel sensor is a matrix of silicon cells. Energy from incoming particles transfers to the material which creates electron-hole pairs that drift towards the collection electrodes. Electrons, under the electric field applied across the reverse biased junction, will drift towards the anode. The hit points are used to reconstruct the trajectories of charged particles, through which basic properties of their momentum and origin can be identified. There are several types of pixel sensors, namely Monolithic, Hybrid planar, and 3D sensors.(8) There are experiments on the LHC like ATLAS and CMS that use hybrid pixel detectors in their tracking systems.(9)

Figure 2 (a) shows the structure of a Hybrid Pixel Detectors (HPD) module. The module consists of a package composed of a sensor and readout chips.(10) Figure 2 (b) shows the structure of a single-pixel cell. It is composed of a pixel sensor connected by bump-bonding process to a CMOS Application Specific Integrated Circuit (ASIC) readout chip for processing and digitizing of signals produced in the pixel sensor also referred to as "Front-End" (FE).(11)

The sensor and FE are fabricated separately due to the incompatibility of the technologies allowing for increased radiation hardness of these two components.(12) The fine segmentation in the pixel sensor improves tracking resolution.(13,14) The pixel modules in the original three layers of the current ATLAS pixel detector were implemented by planar sensors bump-bonded to FE type FE-I3 while, modules in the IBL were implemented with planar and 3D sensors connected to a larger FE type FE-I4.(14)

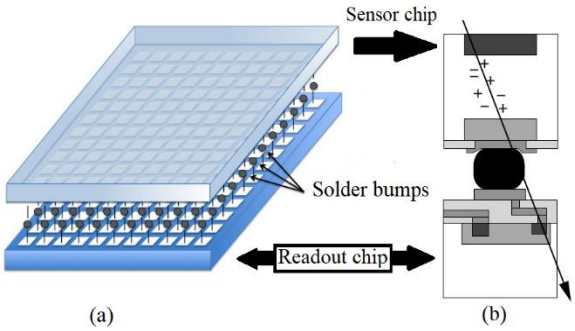


Figure (2): (a): Diagram of a Hybrid Pixel Detector module. (b): Schematic view of a single-pixel cell in a hybrid pixel detector module. Both sensor and a readout chip are separate and electrical connected by a solder bump ball of diameter around 20-30 μm.

ATLAS Internal Tracker for the HL-LHC Upgrade

Figure 3 shows a schematic layout of the future ITk pixel detector. It consists of five layers extending the coverage |η| = 4.(14,16) The ITk pixel detector is divided into three different sub-detectors: the Inner System **(IS)** consisting of the first two layers and their end caps, the Outer Barrel **(OB)** consisting of the three-barrel layers that have two sections: flat and inclined, two Outer Endcaps **(OEs)**, composed of three layers of rings. The ITk has two types of pixel modules that have the same readout chips, but differ in the number of pixels and sensor type. These modules are single chip (one FE chip bump-bonded to a single sensor) and quad (four chips bump-bonded to sensor). Table 1 shows the main difference between these modules.(17)

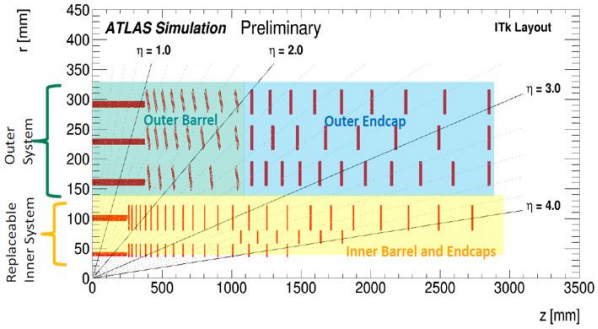


Figure (3): Schematic Layout of ITk pixel detector parts, Layers radii L_0= 39 mm, L_1 =99 mm, L_2 =160 mm, L_3 =220 mm and L_4 =279 mm.

Table (1): ITk Pixel modules types.

Modules	Single Chip	Quad
Size	2 cm × 2 *cm*	4 *cm* × 4 *cm*
Position	First Layer	L_1 to L_4
Sensor type	3D	planar
Pixel Size in μm^2	50 ×50 & 25 ×100	50 ×50

The first pixel detector prototype (ITkPix-V1)

The ITkPix-V1 is a readout Front-End (FE) chip for the ATLAS ITk pixel detector that was developed by RD53 collaboration.(18) The design of ITkPix-V1 is based on 65 nm CMOS technology, it contains a variety of electronic circuits to operate with extreme rates of radiation in ATLAS detector.(19) The chip has three bipolar junction transistors (BJT) sensitive to external radiation in addition to 42 Dose Rate sensors distributed in six banks.(20) The future ITk will be exposed to high radiation levels and high particle density, with an expected Total Ionizing Dose (TID) of approximately 1GRad.(21) The TID signifies the total amount of energy deposited by the ionizing particle that results in electron-hole pairs production, i.e., the limit beyond which the chip gets irreversible damage.(22) The ITkPix-V1 chip must be functional in harsh radiation conditions and endure a wide range of temperature fluctuations, including thermal processes within the range of (-40 ^{0}C to 40 ^{0}C). In order to verify the chip performance and collect lessons for the final version of the Front-End, the ITkPix-V1 is exposed to an ionization dose of 500 MRad to mimic the harsh environment. Figure 4 shows the ITkPix-V1 placed on a Single Chip Card (SCC) board. Table 2

shows the main differences between ATLAS pixel detector readout chips of different versions.(17)

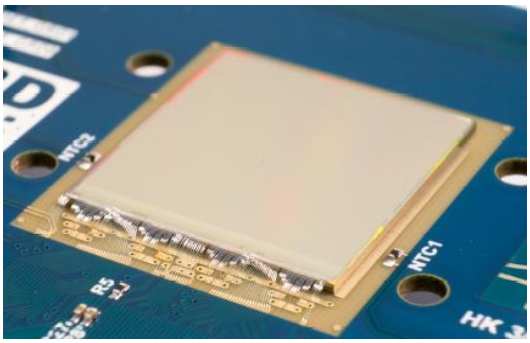


Figure (4): An ITkPix-V1 Front-End readout chip on a single chip card.

Table (2): Different versions of ATLAS pixel detector readout chips.(13, 14, 20)

Chip	FE-I3	FE-I4	ITkPix-V1
Pixel size (μm^2)	50 × 400	50 × 250	50 × 50
Pixels Number	28800	26880	153600
CMOS (nm)	250	130	65
Data rate [Mb/s]	40	320	5120
Radiation Hard	100 MRad	200 MRad	1 GRad

Ring Oscillators

A Ring Oscillator circuit (ROSC) is a combination of CMOS delay stages (NOT gates) connected in a closed-loop with a multiplexer that selects the work mode.(23) Figure 5 shows a diagram of a ROSC consisting of three inverters. ROSCs provide a feedback signal that oscillates at a frequency defined by the number of stages and time delay per stage in such a way to produce a 2π phase shift and must have unity voltage gain at the frequency of oscillation.(24)

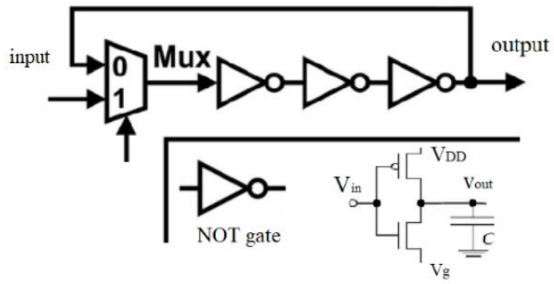


Figure (5): The principle of the Ring Oscillator.

The frequency of the ROSC is given by:

$$f = \frac{1}{2N} \cdot \frac{W}{L} \cdot \frac{\mu C_{OX}(V_{DD} - (V_{t(T_0)} - \alpha(T - T_0)))}{C_L} \cdot \frac{1}{\ln\left(\frac{1.5V_{DD} - 2(V_{t(T_0)} - \alpha(T - T_0))}{0.5V_{DD}}\right)} \quad (1)$$

where, N is the number of NOT gates, (W /L) is the ratio between the width and length of the channel, C_{OX} is the oxide capacitance, C_L is load capacitance, V_t the threshold voltage and μ is the carrier mobility. The temperature dependence of the latter can be estimated by :(25)

$$\mu = \mu_0 \left(\frac{T}{T_0}\right)^{-\frac{3}{2}} \quad (2)$$

As the temperature increases, the mobility and the threshold voltage will both decrease. As a result, the propagation delay will increase leading to a lower ROSC frequency. The change in ROSC frequency is exploited for observing temperature changes.(26) Our approach uses a ROSC as a voltage and temperature sensor since its output frequency depends on the applied voltage and external temperature. By leveraging the voltage and oxide capacitance properties of these circuits, they can serve as an effective benchmark to evaluate the performance of the technology.

Figure 6 shows the block diagram of a single ROSC sensor. It consists of a ROSC circuit connected to a 4-bit counter which counts start/stop cycles output, and a 12-bit counter which counts ROSC clock cycles. In general, ROSC frequency can be calculated by measuring the number of counts and pulse duration.(20)

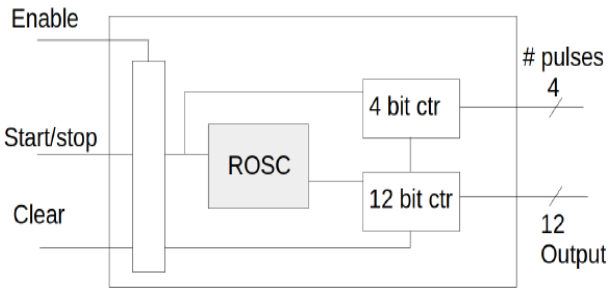


Figure (6): Diagram of a Ring Oscillator block.

The ITkPix-V1 contains a large variety of ROSC sensors. These ROSCs are composed of different kinds and numbers of logic gates and are located in two blocks (ROSCA and ROSCB) within the ITkPix-V1 chip bottom.(20) The ROSCA block contains eight ROSCs, distributed in one bank (Bank A). The ROSCB block contains 32 ROSCs distributed in five banks, which are B-Left, B-Right, LVT, Flip Flop and CAPA. Both Banks, B left and B right, as well as Bank A, contain the same type of ROSCs but with a different number of gates. LVT Bank contains four ROSCs, different in the number of gates. These gates are based on the Low Voltage Threshold of the transistor which is faster than Regular Voltage Threshold gates. The Flip Flop bank contains six oscillators distributed into two parts, Left and Right. Each Flip Flop ring oscillator contains latches that play a crucial role in controlling the oscillation frequency and overall functionality of the oscillator. Bank CAPA contains eight identical ROSCs with each one connected to one injection capacitance as load. Figure 7 shows the names of ROSCs with the number of gates for each one. The two ROSCs blocks are mainly intended to allow for the characterization of logic cell radiation tolerance and redundant measurements on voltage, temperature, and TID.(20)

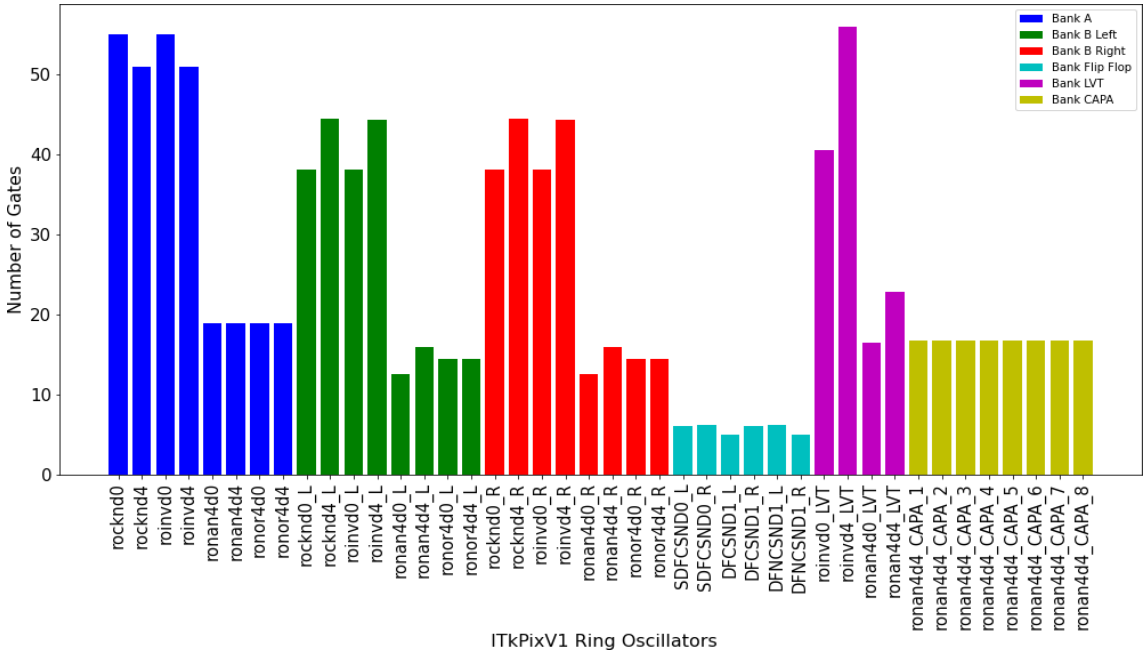


Figure (7): The diagram of the ITkPix-V1 Ring Oscillators names and number of gates for each one.

THERMAL AND SUPPLY VOLTAGE TEST OF THE ITKPIX-V1 CHIP

This work aims at studying the performance of the ITkPix-V1 read-out chip and validate the ability of the readout circuit to fulfill the future ATLAS Pixel operating requirements by simulating the harsh radiation environment of the HL-LHC. Generally, during data taking, the readout chip temperature can increase due to power dissipation in the electronics, estimated by W/cm^2. For this reason, the future ITk will be locally cooled by CO_2 cooling tubes. In addition, CO_2 cooling is necessary to avoid reverse annealing of the sensors and control the leakage current in heavy radiation-damaged silicon.(27) Therefore, it is important to evaluate the impact of temperature change on readout chips through the frequency variation of ROSCs. The ITkPix-V1 chip was tested by varying the applied voltage while modifying the external temperature with the use of a climate chamber.

Voltage Dependence

To characterize the dependency of the ROCS frequency in terms of supply voltage VDDD, the ITk ITkPix-V1 chip was tested using two special readout boards; the Single Chip Card (SCC), where the ITkPix-V1 chip is wire-bonded on, and BDAQ53 a readout board for lab-test of ATLAS pixel modules. The BDAQ53 establishes a connection between the computer and SCC to acquire and collect data from the chip. The BDAQ53 system is a Python-based Data Acquisition System (DAQ) specifically designed for chip testing purposes.(28) The SCC is supplied with equal digital (VIND) and analog (VINA) voltage values, 1.6 V on both inputs, as shown in the figure 8.

These voltages are reduced and regulated using the internal Shunt Low Drop Out (SLDO) regulator (constant current) to power the ROSCs, with two different input voltages, one analog (VDDA) and one digital (VDDD). For that, the chip takes a constant current with a value of approximately 0.5 A, and the user varies the voltage to the digital power domain. The voltage values were taken in a range between 0.975 V to 1.4 V to be around the real value of 1.2 V, which is used for the actual experiments. For each voltage value, frequency values are read from all ROSCs. Figure 9 shows the digital voltage dependency of the measured frequency for all ROSCs. The frequencies show a linear variation with VDDD. We note that the frequencies increase with VDDD increase. The ROSCs that have the same or approximately same number of gates (like in figure 7) present similar frequency versus voltage tendencies (like in figure 9).

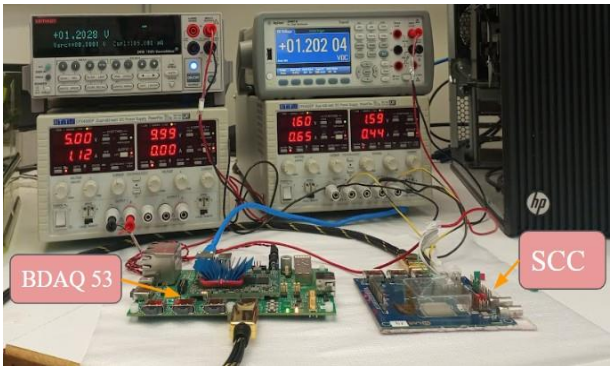


Figure (8): Voltages measurement extracted through two digital multimeters.

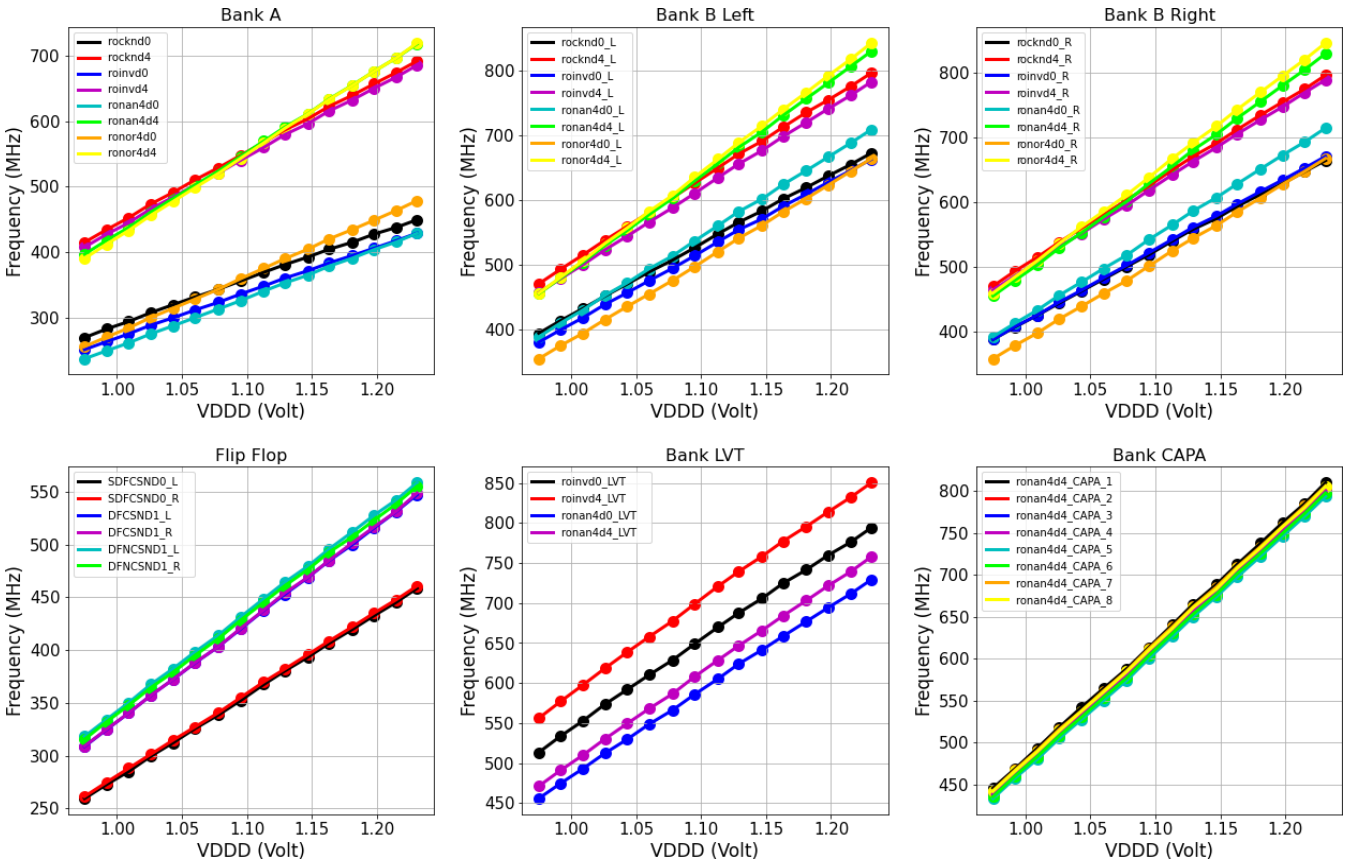


Figure (9): ITkPix-V1 Ring Oscillators frequencies versus applied Digital Voltage VDDD for all banks at room temperature.

Temperature Dependence

To study the frequency of ROSC dependency on temperature, we use the same setup previously presented, but the ITkPix-V1 chip is placed within a climatic chamber as shown in figure 10. The ROSCs frequencies were registered versus temperature values ranging from -40 ^{0}C to 40 ^{0}C with 10 ^{0}C steps, while the voltage was regulated at 1.2 V at all temperature values. Figure 11 shows the results of the frequency variation as a function of temperature. It demonstrates the expected dependence of ROSC frequency on temperature changes, as predicted by the mobility factor in equation (1). As the mobility decreases, the frequency increases due to the exponential behavior of the mobility concerning temperature. Consequently, with increasing temperature, one can observe a decrease in the oscillator frequency. In the range from -40 ◦C to 40 ◦C, it is not quite linear, the curves are approximately straight line and curvy for all banks. The sensitivity of ROCS can vary depending on environmental factors, including supply voltage variations, process fluctuations, and electromagnetic interference.

These factors can significantly impact the accuracy of the sensor. Moreover, the sensitivity to temperature changes may not be reliable outside a specific temperature range, necessitating precise calibration to ensure accurate measurements. To ensure reliable and accurate readings, it is essential to consider a valid temperature range for the sensor's operation. In certain temperature ranges, the ROCS can function as a temperature sensor, offering additional utility in temperature monitoring applications.

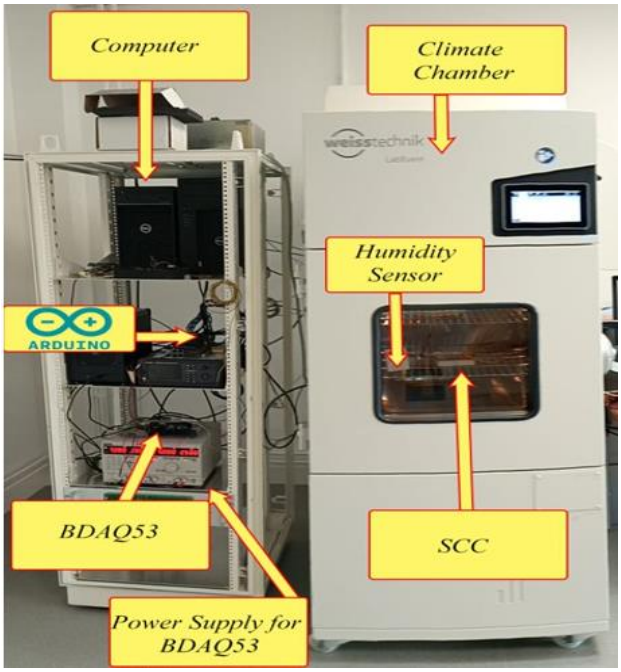


Figure (10): ITkPix-V1 Front-End Chip on SCC inside the climate chamber (Heraeus HT4020) in addition to other devices that had been used in the IJC-Lab.

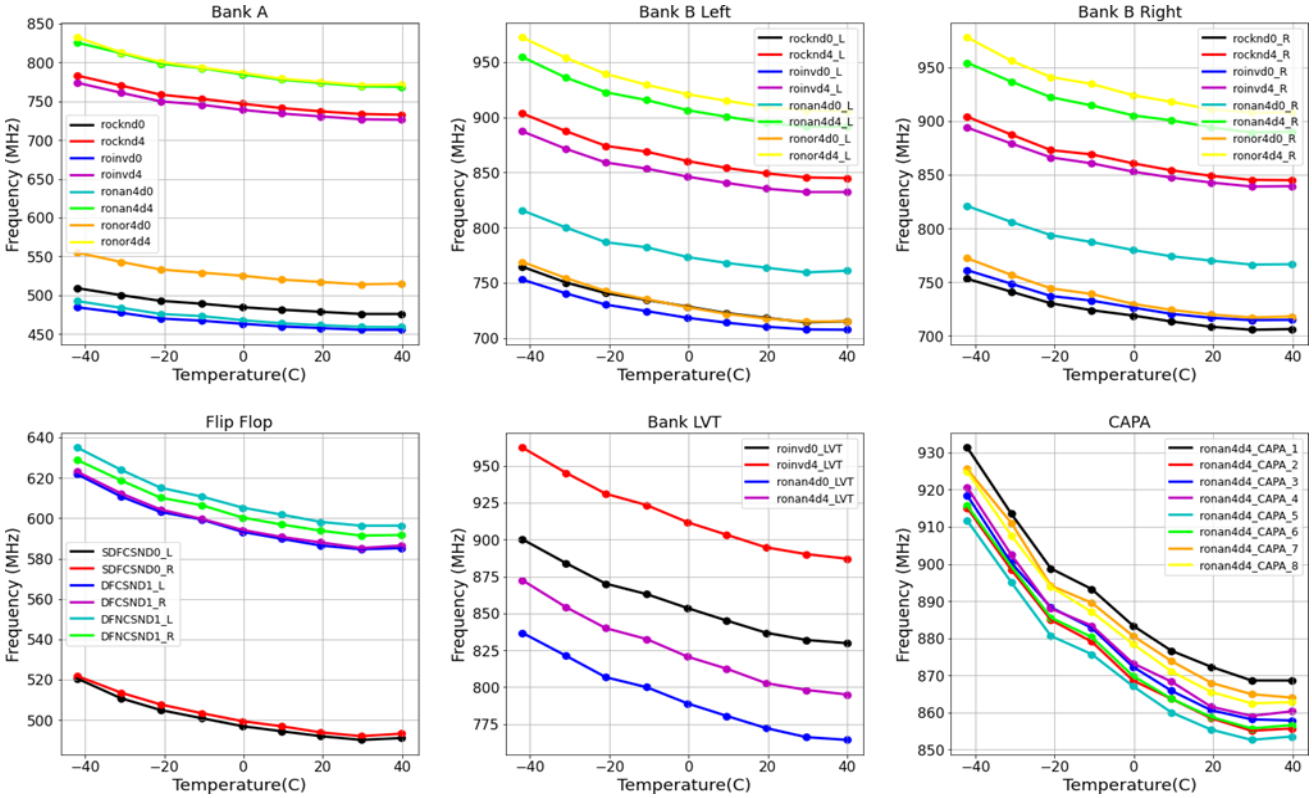


Figure (11): The Ring Oscillators Frequencies versus Temperature. The temperature was measured on the chip surface. In the climate chamber the temperature was changed from -40 ^{0}C to 40 ^{0}C.

Conclusion

The proposed ATLAS ITk upgrade for HL-LHC will be implemented using hybrid pixel modules bump-bonded to a 65 nm CMOS ASIC. The ITkPix-V1 chip contains 42 ROSCs with different logic gates that allow for increased redundancy and studies of different configurations.

The experimental results demonstrate that the frequency of the ROSC increases linearly as digital voltage increases, while it decreases as temperature increases. The thermal and supply voltage experimental setup of our experiment is working well and the ITkPix-V1 shows good performance during the process and looks roughly as expected.

This study was carried out on the embedded ROSCs inside the ITkPix-V1 Front-End ATLAS chip and has proven that it could be used as a reliable temperature sensor through its frequency response to temperature changes. However, the sensitivity and uncertainty determination needs further studies and investigation. Frequency response of the ROSC scales linearly with digital voltage input providing a very sensitive way to prove fluctuation of the supply voltage in the readout circuitry. The frequency measurements of the ROCS's voltage and temperature show that the implemented ITk modules with the ITkPix-V1 chips will be suitable for the HL-LHC era.

Ethics approval and consent to participate

The authors confirm that they respect the publication ethics and that they consent the publication of their work.

Consent for publication

The authors consent the publication of this work. Availability of data and materials Data is available upon the request.

Author's contribution

The results presented here are mainly based on the original idea from A.Lounis, H. Abualrob and A. Bassalat as well their conceptualization. Full Analysis Carried by O.Istaitia and Y.Khwaira. The original draft had been produced by O. istaitia. Experimental support by A.Slimani-Cherif and M.Cohen-Solal.

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Conflicts of interest

All authors declare that they have no conflicts of interest.

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